REMARKS

Applicant has reviewed and considered the Office Action mailed on July 16, 2003 and the Advisory Action mailed on October 9, 2003, and the references cited therewith.

Claims 13 and 14 are amended, no claims are canceled, and no claims are added; as a result, claims 13-18 and 26-45 are now pending in this application. The amendments to the claims are fully supported by the specification as originally filed. No new matter is introduced. Applicant respectfully requests reconsideration of the above-identified application in view of the amendments above and the remarks that follow.

The amendment to claim 13 will place it in condition for allowance in which the amendment includes limitations in line with the allowable subject matter of claim 34. Claim 14 is amended to follow the language of claim 13.

Claim 13 finds support in the specification, for example, on page 5, lines 7-17.

First §103 Rejection of the Claims

Claims 13-16 were rejected under 35 USC § 103(a) as being unpatentable over Okamura (U.S. 5,521,541) in view of Chi (U.S. 5,387,885) and Sano et al. (JP 2-158165). Applicant traverses these rejections.

Applicant respectfully submits that the Office Action did not make out a proper *prima facie* case of obviousness for at least the following reasons:

(1) there is no suggestion to combine the cited references, and

(2) even if combined, the cited references fail to teach or suggest all of the elements of applicant's claimed invention.

The Office Action stated

> "In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a signal wiring pattern having sufficiently low losses) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns,* 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)."

Applicant respectfully notes that the Examiner has misinterpreted Applicant's previous response.

Applicant's previous response did not discuss Applicant's claims. Instead, the response was directed to pointing out that the combination of cited references Okamura and Chi was not proper, and therefore, the Office Action did not present a proper *prima facie* case of obviousness. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143.

The cited references and the current Office Action do not provide a teaching or suggestion to make the combination of Okamura with Chi or a reasonable expectation of success for the proposed combination. Chi appears to require a lossless medium, at least a slightly lossy medium for a salphasic distribution, dealing mainly with lossless or slightly lossy medium at the system level, for example at the printed circuit board level and higher in system hierarchy. Further, Chi recites at column 10, lines 6-10,

> "[t]he design methodology of the present invention is, therefore, to provide a distribution system which exhibits salphasic behavior. According to this methodology, the following three conditions must be met.
> First, the propagating medium (for example, the branches of the tree network shown in FIG. 6) must be substantially lossless and bounded."

Applicant can not find a teaching or suggestion in Okamura for a signal wiring pattern having sufficiently low losses to make salphasic clocking feasible. Thus, Applicant submits that there is no teaching or suggestion for combining Okamura and Chi. Therefore, since the combination is not proper, there is no basis to make a comparison with Applicant's claims.

Further, Sano et al. (hereafter Sano) appears to deal with a method and structure to suppress signal leakage between channels (*See Sano Abstract)* and does not appear to provide a teaching or suggestion that cures the abovementioned deficiencies in combining Okamura and Chi.

However, to expedite prosecution of the instant application, Applicant amends claim 13. Applicant can not find in the combination of Okamura and Chi with Sano, a teaching or suggestion of a clock signal distribution network including an on-die interconnect section having two differential signal lines structured as recited in claim 13, as amended, to reduce inductance

losses with a signal return path. Though the combination of Okamura and Chi is not proper, even if, arguendo, Okamura and Chi are combined with Sano, the combination does not teach or suggest all the elements of claim 13, and thus, would not make a proper *prima facie* case of obviousness with respect to claim 13.

Therefore, for the abovementioned reasons, claim 13 is patentable over Okamura, Chi, and Sano. Claims 14-16 are dependent on claim 13 and are patentable for the reasons stated above, and additionally in view of the further elements recited in these dependent claims.

Applicant requests withdrawal of these rejections of claims 13-16, and reconsideration and allowance of these claims.

Second §103 Rejection of the Claims

Claims 17, 18 and 26 were rejected under 35 USC § 103(a) as being unpatentable over Okamura in view of Chi, Sano et al. and Restle et al. (IEEE Symposium on VLSI Circuits Digest of Technical Papers, pp. 2-5 (1998)). Applicant traverses these rejections.

Adding Restle et al. (hereafter Restle) to the combination of patents cited in the above rejection does not cure the deficiencies of the rejection of claim 13 based on Okamura, Chi, and Sano, as discussed above. Claims 17, 18, and 26 are dependent on claim 13 and are patentable for the reasons stated above, and additionally in view of the further elements recited in these dependent claims.

Applicant requests withdrawal of these rejections of claims 17, 18, and 26, and reconsideration and allowance of these claims.

Allowable Subject Matter

Claims 27-45 were allowed.

Applicant acknowledges allowance of claims 27-45.

Assertion of Pertinence

Applicant has not responded to the assertion of pertinence stated for the patents cited but not relied upon by the Office Action since these patents are not relied upon as part of the

rejections in this Office Action. Applicant is expressly not admitting to any assertion of their pertinence and reserves the right to address the assertion should it form a part of some future rejection.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 371-2157 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15 day of October, 2003

Anne M. Richards

Name

Signature

IN THE CLAIMS

Please amend the claims as follows:

1-12. (Canceled)

13. (Currently Amended) A microelectronic die comprising:

a clock signal source to provide a clock signal; and

a clock signal distribution network to distribute said clock signal to multiple clocked elements within said microelectronic die using salphasic clocking techniques, said clock signal distribution network including at least one on-die interconnect section comprising first and second differential signal lines on a first metal layer of said microelectronic die to carry a differential version of said clock signal, said first and second differential signal lines being substantially parallel to one another, wherein the first and second differential signal lines each have widths such that the widths and a spacing between the first and second differential signal lines are selected to reduce inductance losses with a signal return path on a second metal layer of said microelectronic die.

14. (Currently Amended) The microelectronic die of claim 13, comprising:

at least one trace on [[a]] the second metal layer of said microelectronic die, said at least one trace being capacitively coupled to and non-parallel with said first and second differential signal lines.

15. (Original) The microelectronic die of claim 14, wherein:

said at least one trace is substantially orthogonal to said first and second differential signal lines.

16. (Original) The microelectronic die of claim 13, wherein:

said clock signal is sinusoidal.

17. (Original) The microelectronic die of claim 13, wherein:

said first and second differential signal lines are part of a clock grid within said clock distribution network.

18. (Original) The microelectronic die of claim 13, wherein:

said first and second differential signal lines are part of an H-tree within said clock distribution network.

19-25. (Canceled)

26. (Previously Presented) The microelectronic die of claim 13, wherein said microelectronic die includes microprocessor circuitry.

27. (Previously Presented) A microelectronic die comprising:

a clock signal source to provide a clock signal; and

a clock signal distribution network to distribute the clock signal to multiple clocked elements within the microelectronic die using salphasic clocking techniques, the clock signal distribution network including a number of on-die interconnect sections having first and second differential signal lines on a first metal layer of the microelectronic die to carry a differential version of the clock signal, the first and second differential signal lines being substantially parallel to one another; and

a number of conductive links, wherein a first conductive link of the number of conductive links couples the first differential signal line of a first one of the interconnect sections to the first differential signal line of a second one of the interconnect sections and a second conductive link of the number of the conductive links couples the second differential signal line of the first one of the interconnect sections to the second differential signal line of the second one of the interconnect sections.

28. (Previously Presented) The microelectronic die of claim 27, wherein said microelectronic die includes microprocessor circuitry.

29. (Previously Presented) The microelectronic die of claim 27, wherein the multiple clocked elements are coupled to the clock distribution network at locations where the clock signal has a signal phase independent of the position of the locations.

30. (Previously Presented) The microelectronic die of claim 27, wherein the clock signal distribution network includes a salphasic clock gird in which the clock signal has a signal phase that is substantially position independent for the entire salphasic clock gird.

31. (Previously Presented) The microelectronic die of claim 27, further including a number of traces on a second metal layer of the microelectronic die, the number of traces being capacitively coupled to and non-parallel with the first and second differential signal lines.

32. (Previously Presented) The microelectronic die of claim 31, wherein the number of traces are substantially orthogonal to the first and second differential signal lines.

33. (Previously Presented) The microelectronic die of claim 31, wherein the number of traces includes signal lines or power lines.

34. (Previously Presented) A microelectronic die comprising:

a clock signal source to provide a clock signal; and

a clock signal distribution network to distribute the clock signal to multiple clocked elements within the microelectronic die using salphasic clocking techniques, the clock signal distribution network including an on-die interconnect section having first and second differential signal lines on a first metal layer of the microelectronic die to carry a differential version of the clock signal, the first and second differential signal lines, having a resistance per unit length,

being substantially parallel to one another with a spacing between the first and second differential signal lines; and

a number of traces on a second metal layer of the microelectronic die, the number of traces being capacitively coupled to and non-parallel with the first and second differential signal lines providing a high inductance return path to the clock signal propagating on the first and second differential, the high inductance return path having an inductance per unit length, wherein a width for each of the first and second differential signal lines and the spacing between the first and second differential signal lines are selected to decrease loss by decreasing a ratio of the resistance per unit length to the inductance per unit length.

35. (Previously Presented) The microelectronic die of claim 34, wherein the number of traces are substantially orthogonal to said first and second differential signal lines.

36. (Previously Presented) The microelectronic die of claim 34, wherein the clock signal is sinusoidal.

37. (Previously Presented) The microelectronic die of claim 34, wherein the first and second differential signal lines are part of a clock grid within the clock distribution network.

38. (Previously Presented) The microelectronic die of claim 34, the first and second differential signal lines are part of an H-tree within said clock distribution network.

39. (Previously Presented) The microelectronic die of claim 34, wherein the multiple clocked elements are coupled to the clock distribution network at locations where the clock signal has a signal phase independent of the position of the locations.

40. (Previously Presented) The microelectronic die of claim 34, wherein the clock signal distribution network includes a salphasic clock gird in which the clock signal has a signal phase that is substantially position independent for the entire salphasic clock gird.

41. (Previously Presented) The microelectronic die of claim 34, further including a number of on-die interconnect sections having first and second differential signal lines and a number of conductive links, wherein a first conductive link of the number of conductive links couples the first differential signal line of a first one of the interconnect sections to the first differential signal line of a second one of the interconnect sections and a second conductive link of the number of the conductive links couples the second differential signal line of the first one of the interconnect sections to the second differential signal line of the second one of the interconnect sections.

42. (Previously Presented) The microelectronic die of claim 34, wherein the clock signal distribution network includes a salphasic clock gird having a number of locations at which the clock signal is fed to the salphasic clock gird.

43. (Previously Presented) The microelectronic die of claim 42, further including buffer units at the number of locations, the buffer units having small, differential outputs to drive the clock signal.

44. (Previously Presented) The microelectronic die of claim 42, wherein the salphasic clock gird provides the clock signal having a signal phase that is substantially position independent for the entire salphasic clock gird.

45. (Previously Presented) The microelectronic die of claim 42, wherein the clock signal distribution network includes a salphasic clock gird in which the clock signal has a signal phase that is substantially position independent for the entire salphasic clock gird.